Hall Ticket Number:

Code No. : 17444 S (A) N/O

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) VII-Semester Supplementary Examinations, May/June-2023

Field Programmable Gate Arrays Architectures (PE-III)

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Q. No.	Stem of the question	M	L	CO	PO
	Part-A (10 × 2 = 20 Marks)				
1.	Distinguish between PLA and PAL.	2	4	1	2
2.	What are different FPGA programming Technologies?	2	1	1	1,2
3.	List the applications of FPGA.	2	1	2	1,2
4.	What are the dedicated specialized components of FPGAs?	2	1	2	1,2
5.	Write the salient features of Altera FPGAs.	2	2	3	1
6.	Compare the logic blocks of Vertex-II and Spartan-II FPGAs.	2	4	3	2
7.	What is the significance of placement in FPGA design?	2	4	4	1,2
8.	Write briefly about Net delays.	2	1	4	1
9.	Mention various steps in FPGA implementation?	2	2	5	1,2
10.	Discuss the importance of fault coverage for any testing method.	2	4	5	3,4
	Part-B (5×8 = 40 Marks)				
11. a)	Design a full adder circuit with PLA.	3	3	1	2,3
b)	Explain the flow diagram of FPGA design.	5	2	1	2
12. a)	Draw and explain the general block diagram of FPGA.	4	2	2	1
b)	Explain how the performance of FPGA depends on the functionality of logic block.	4	4	2	2
13. a)	Draw the block diagram for Xilinx XC4000 series logic block and explain the functionality.	4	2	3	3,4
b)	What are the architectural difference between ACT2 and ACT3 FPGAs? Compare their performance.	4	4	3	3,4
14. a)	Explain Mincut based placement algorithm.	4	2	4	2,3
b)	With the help of an example explain the Maze routing algorithm.	4	3	4	2,3
15. a)	What is design validation? Explain its importance in FPGA design.	4	4	5	2,5
b)	Explain ATPG methods in detail.	4	2	5	3,5
16. a)	What are Sequential PLDs? What are the applications of Sequential PLDs?	4	1	1	1
b)	Explain why SRAM based FPGAs are popular when compared to other types?	4	4	2	2
17.	Answer any ***two*** of the following:				
a)	What is routing architecture? Explain in detail.	4	2	3	4,5
b)	Explain the Simulated Annealing for Placement.	4	2	4	3
c)	Write short notes on EDA tools.	4	1	5	5

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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